Amendments to the Drawings

The attached sheet of drawings includes changes to Fig. 5A. This sheet, which includes Fig. 5A, replaces the original sheet including Fig. 5A. In Figure 5A, a spread spectrum control circuit 50 is depicted, and the label of block 52 is corrected as "phase modulator" to comply with the related descriptions of the specification. No new matter is introduced.

Attachment: Replacement Sheet

REMARKS

Claims 17-39 stand rejected. As set forth above, claims 32-39 have been cancelled without prejudice. Accordingly, claims 17-31 currently are pending in this application. Favorable reconsideration and allowance of the pending claims are respectfully requested.

Response to the drawing objections:

Fig. 5A is amended to show a spread spectrum control circuit 50 without entering any new matters. The label of block 52 in Fig. 5A is also corrected to be "phase modulator", so as to comply with the related descriptions of the specification. Besides, the frequency control circuit as recited in claim 17 could be found by the phase modulator 52 of Fig. 5A, which couples to the multi-phase oscillation clock generator 51 and the modulation value generator 54, for generating the modulation clock signal according to the oscillation clock signal and the modulation value with which an average frequency of the modulation clock signal varies. Therefore, the current drawings have shown every feature of the invention specified in the claims.

Response to the claim rejections:

Claims 17 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyabe et al. (U.S. Patent No. 6,559,698). Specifically, the current Office action stated:

> Regarding claims 17, 25 and 32:
>
> As shown in figures 1, Miyabe et al. discloses a clock generating circuit, comprising:

a clock generator (1 in figure 1) for receiving a reference clock signal (4 in figure 1) and thereby generating an output clock signal (14 in figure 1); and

a spread spectrum control circuit (clock modulation circuit is interpreted to be the spread spectrum control circuit) (2 in figure 1), coupled to the clock generator (1 in figure 1), for generating a modulated clock signal with frequency variation (19, a in figure 1) according to the output clock signal and a modulation value (column 5, lines 16-32), comprising:

a modulation value generating circuit (19 in figure 1) for outputting the modulation value (a in figure 1); and

a frequency control circuit (15 in figure 1), coupled to the clock generator (1 in figure 1) and the modulation value generating circuit (19 in figure 1), for generating the modulated clock signal according to the output clock signal (14 in figure 1) and the modulation value (19, a in figure 1) with which an average frequency of the modulated clock signal varies (column 5, lines 57-67, and column 6, lines 1-29);

wherein the clock generator operates in a way being independent of the spread spectrum control circuit, and the modulation value varies with time in a predetermined manner so as to force the average frequency of the modulated clock signal to change up and down over time (column 5, lines 57-67, and column 6, lines 1-29).

(Emphasis added)

Applicant asserts that claim 17 is patentable over Miyabe et al. because Miyabe et al. at least fail to teach or suggest the following limitations: "wherein the clock generator operates in a way independent of the spread spectrum control circuit". The current Office action stated that the 2nd order PLL system 1 and the clock modulating circuit 2 of

Miyabe et al. respectively disclose the claimed clock generator and the spread spectrum control circuit. However, with respect to figure 1 and related descriptions of Miyabe et al., it is clearly shown that **the 2nd order PLL system 1 operates in accordance with the output signal 24 from the clock modulating circuit 2**, so as to generate the output clock signal 14 (Miyabe et al.: Fig. 1; Col. 5, line 57 – Col. 6, line 29). This teaching obviously is contrary to the above-mentioned limitations. The specification of this application mentions this claimed feature, which recites: "It is therefore one of the objects of the invention to provide a phase lock loop circuit using phase modulation technology, wherein **a modulation signal does not have to be used in the PLL of the circuit**, so the capacitor area of the loop filter in the PLL does not have to be enlarged and the size of the circuit device may be effectively reduced." (Specification: Paragraph [0009]). Therefore, Miyabe et al. fail to disclose all the claimed limitations of claim 17, and thereby claim 17 is in condition of allowance. Since claims 18-24 are dependent upon claim 17, if claim 17 is found to be allowable, so too should the dependent claims.

Applicant also asserts that claim 25 is patentable over Miyabe et al. based on the same reasons placing claim 1 allowable. Claim 25 recites the following limitations: "wherein the output clock signal is generated in a way being independent of the spread spectrum control step". Miyabe et al. at most disclose the 2nd order PLL system 1 generates an output clock signal 14 according to the output signal 24 from the clock modulating circuit 2 (Miyabe et al.: Fig. 1; Col. 5, line 57 – Col. 6, line 29), but nowhere teach or suggest the output clock signal 14 generated in a way being independent of the clock modulating circuit 2. Therefore, Miyabe et al. fail to disclose all the limitations of claim 25, and thereby claim 25 is in condition of allowance. Since claims 26-31 are dependent upon claim 25, if claim 25 is found to be allowable, so too should the dependent claims.

Conclusion:

Therefore, all pending claims are submitted to be in condition for allowance. Applicants respectfully request a timely notice of allowance be issued in this case. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)